Japan Display Inc.

FOR MESSRS: _____ DATE : Feb. 1st, 2023

CUSTOMER'S ACCEPTANCE SPECIFICATIONS

ADB31200

Contents

No.	ITEM	SHEET No.	PAGE
1	COVER	7B64PS 2701-ADB31200-2	1-1/1
2	RECORD OF REVISION	7B64PS 2702-ADB31200-2	2-1/1
3	GENERAL DATA	7B64PS 2703-ADB31200-2	3-1/2~2/2
4	ABSOLUTE MAXIMUM RATINGS	7B64PS 2704-ADB31200-2	4-1/1
5	ELECTRICAL CHARACTERISTICS	7B64PS 2705-ADB31200-2	5-1/1
6	BLOCK DIAGRAM	7B64PS 2706-ADB31200-2	6-1/1
7	INTERFACE	7B64PS 2707-ADB31200-2	7-1/3~3/3
8	OUTLINE DIMENSIONS	7B64PS 2708-ADB31200-2	8-1/1
9	DESIGNATION OF LOT MARK	7B64PS 2709-ADB31200-2	9-1/1

ACCEPTED BY : _____ PROPOSED BY : Oblack Tsai

2. RECORD OF REVISION

DATE	SHEET NO.	SUMMARY
Feb.01,'23	7B64PS 2701-ADB31200-2 Page 1-1/1	Company logo changed : KOE JDI Group Kaohsiung Opto-Electronics Inc. → JDI Japan Display Inc.
	7B64PS 2709-ADB31200-2 Page 9-1/1	
	All page	Company name changed: From "JDI Taiwan Inc. Kaohsiung Branch" to "JDI Taiwan Inc. Kaohsiung Branch"

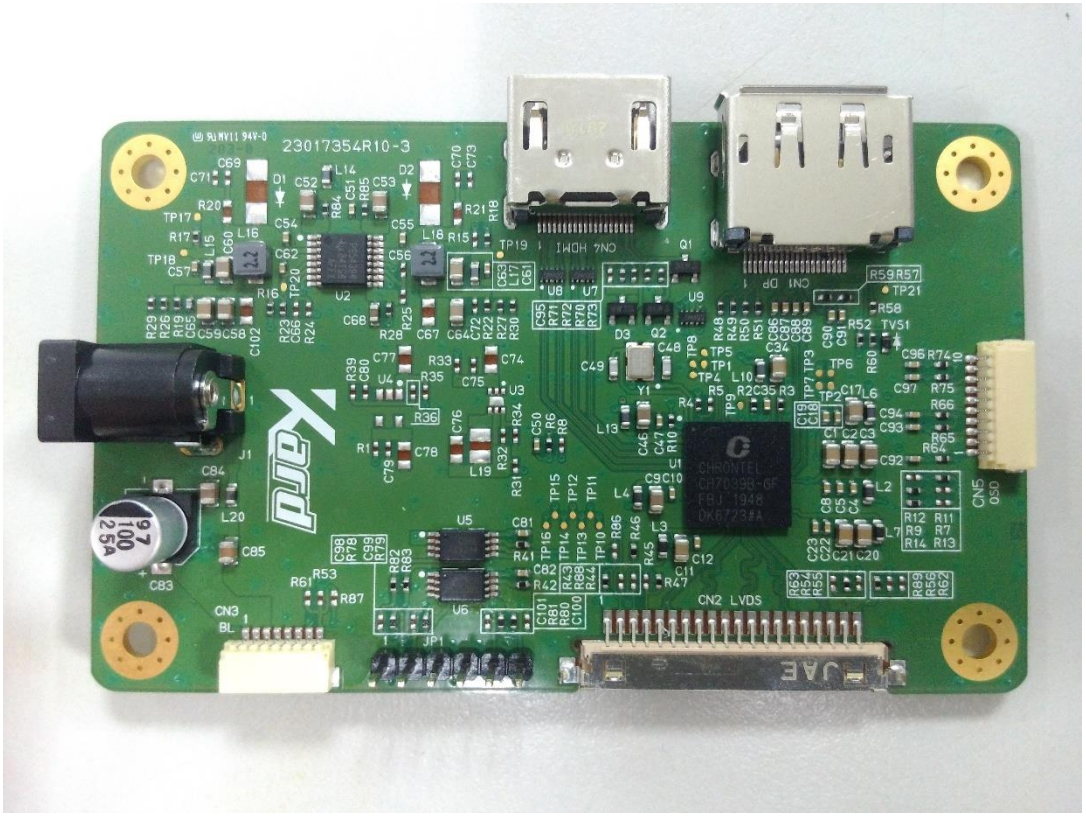
3. GENERAL DATA

3.1 FEATURES

It is a bridge board specification for TFT driving, this Bridge board is designed for TX31D2D00 module (made by Kaohsiung Opto-Electronics). This bridge board is RoHS compliant.

Part Name	ADB31200
Module Dimensions	55.0(W) mm x 90.0(H) mm x 14.5(D) mm (except OSD board & cable)
Resolution	1280 x 3(RGB)(W) x 480(H) Dots
Number of Colors	16.7M Colors (8-bits RGB)
Input Interface	HDMI:19 pins; Display Port: 20 pins
Output Interface	LVDS; 20 pins
Input Voltage	12 V
Input Current	2A
Weight	36 g

3.2 ACKAGE CONTENTS

Part Name	Quantity
 Bridge Board	1
 OSD Board	1
 OSD Cable	1

4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remarks
Input Supply Voltage	V_{IN}	-0.3	16	V	
Input Supply Current	I_{IN}	-	2	A	
Operating Temperature	T_{op}	0	70	˚C	Note 1
Storage Temperature	T_{st}	-20	70	˚C	Note 1

Note 1: The maximum rating is defined as above based on the chamber temperature, which might be different from ambient temperature after assembling the panel into the application.

5. ELECTRICAL CHARACTERISTICS

5.1 INPUT DC SPECIFICATIONS

$T_a = 25\ ^{\circ}C,\ V_{SS} = 0V$

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V_{IN}	11.4	12.0	12.6	V	-
Power Supply Current	I_{IN}	-	-	1750	mA	Note1

Note 1: Maximum current is measured by heavy loading pattern based on V_{IN}=12V.

5.2 INPUT HDMI RECEIVER SPECIFICATIONS

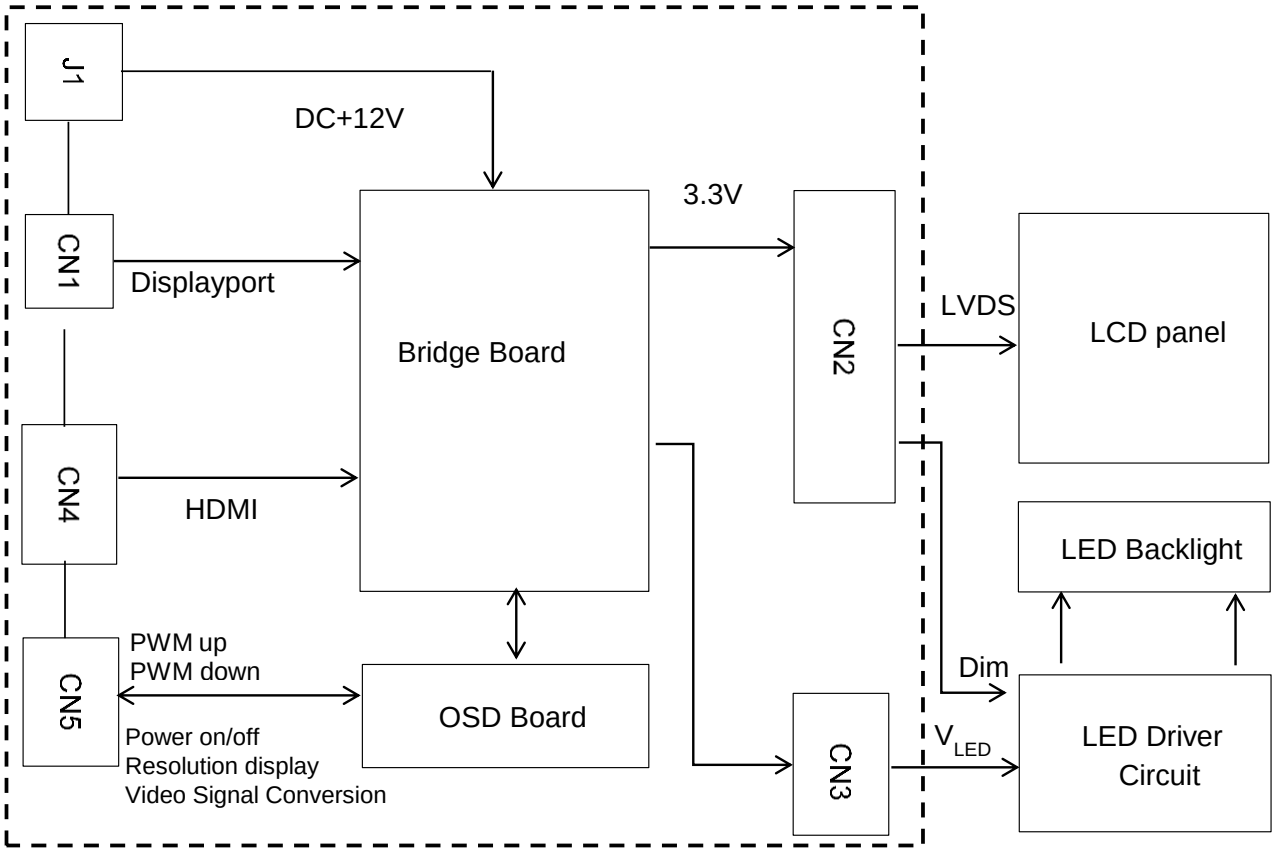
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Intra-Pair (+ to -) Differential Input Skew	T_{DPS}	-	-	0.4	T_{bit}	-
Channel to Channel Differential Input Skew	T_{CCS}	-	-	10	T_{bit}	-
Differential Input Clock Jitter Tolerance	T_{IJIT}	-	-	0.3	T_{bit}	-
TMDS CLK Frequency (HDMI mode)	F_{RXC}	25	-	165	MHz	-

5.3 INPUT DP RECEIVER SPECIFICATIONS

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Unit Interval for High Bit Rate (2.7Gbps/lane)	UI_{High_Rate}	-	370	-	ps	Note1
Unit Interval for High Bit Rate (1.62Gbps/lane)	UI_{High_Rate}	-	617	-	ps	Note1
Minimum Receiver Minimum Eye Width at Rx-side connect pins	$t_{RX\text{-}EYE_CONN}$	0.51	-	-	UI	-
Minimum Receiver Minimum Eye Width at Rx package pins	$t_{RX\text{-}EYE_CONN}$	0.47	-	-	UI	-
Maximum time between the jitter median and maximum deviation from the median at Rx package pins	$T_{RX\text{-}EYE\text{-}MEDIANto\text{-}MAX\text{-}ITTER_CHIP}$	-	-	0.265	UI	-
Lane-to-Lane Skew at RX package pins	$L_{RX\text{-}SKEWINTER_PAIR}$	-	-	5200	ps	-
Lane Intra-pair Skew at RX package pins	$L_{RX\text{-}SKEWINTRA_PAIRHigh\text{-}Bit\text{-}Rate}$	-	-	100	ps	-
Lane Intra-pair Skew at RX package pins	$L_{RX\text{-}SKEWINTRA_PAIR_Reduced\text{-}Bit\text{-}Rate}$	-	-	300	ps	-
Jitter Tracking Bandwidth	$F_{RX\text{-}TRACKINGBW}$	20	-	-	MHz	-
AUX Unit Interval	UI	0.4	0.5	0.6	us	-
Number of pre-charge pulse	$T_{AUX\text{-}BUS\text{-}Pre\text{-}charge}$	10	-	16	-	-
AUX CH bus park time	$T_{AUX\text{-}BUS\text{-}PARK}$	10	-	-	ns	-
Cycle-to-cycle jitter at Receiver Package pins	$T_{cycle\text{-}to\text{-}cycle\ jitter}$	-	-	0.05	UI	-

Note 1: Test condition: Range is nominal +/-350ppm.

6. BLOCK DIAGRAM



7. INTERFACE

7.1 INPUT PIN ASSIGNMENT

The interface connector (J1) is CDD-04PB-020 made by FLYiNG or equivalent connector and pin assignment is as below:

Item	Pin No.	Signal	Function
J1	1	Vin(12V)	Power supply for driving
	2	GND	GND
	3	GND	GND

The interface connector (CN1) for DP is G3167-03010111-H0 made by Wieson or equivalent connector and pin assignment is as below:

Item	Pin No.	Signal	Function
CN1 (DP)	1	ML_Lane3(n)	Lane 3 (negative)
	2	V_{SS}	GND
	3	ML_Lane3(p)	Lane 3 (positive)
	4	ML_Lane2(n)	Lane 2 (negative)
	5	V_{SS}	GND
	6	ML_Lane2(p)	Lane 2 (positive)
	7	ML_Lane1(n)	Lane 1 (negative)
	8	V_{SS}	GND
	9	ML_Lane1(p)	Lane 1 (positive)
	10	ML_Lane(n)	Lane (negative)
	11	V_{SS}	GND
	12	ML_Lane(p)	Lane (positive)
	13	V_{SS}	GND
	14	V_{SS}	GND
	15	AUX_CH(p)	Auxiliary Channel (positive)
	16	V_{SS}	GND
	17	AUX_CH(n)	Auxiliary Channel (negative)
	18	Hot Plug	Hot Plug Detection
	19	DP_PWR (Return)	GND
	20	DP_PWR	No Connection

The interface connector (CN4) for HDMI is 2086581001 made by Molex or equivalent connector and pin assignment is as below:

Item	Pin No.	Signal	Function
CN4 (HDMI)	1	DATA 2+	TMDS Date 2+
	2	GND	TMDS Data 2 shield
	3	DATA 2-	TMDS Data 2-
	4	DATA 1+	TMDS Data 1+
	5	GND	TMDS Data 1 shield
	6	DATA 1-	TMDS Data 1-
	7	DATA 0+	TMDS Data 0+
	8	GND	TMDS Data 0 shield
	9	DATA 0-	TMDS Data 0-
	10	CLOCK+	TMDS Clock+
	11	GND	TMDS Clock shield
	12	CLOCK-	TMDS Clock-
	13	CEC	Not Connected
	14	Reserved	Not Connected
	15	SCL	Serial Clock for DDC
	16	SDA	Serial Data Line for DDC
	17	GND	DDC / CEC / HEC Ground
	18	VDD(+5V)	Power supply for logic
	19	HPDET	Hot plug detect

The clicker (CN5) assignment for OSD (On Screen Display) is as below:

Item	Pin No.	Signal	Function
CN5	SW1	PWM UP	Brightness dimming
	SW2	PWM DOWN	Brightness dimming
	SW3	POWER On/Off	Display On/Off control
	SW4	Resolution Display	Resolution information
	SW5	Video Signal Conversion	Scan direction control

7.2 OUTPUT PIN ASSIGNMENT

The display interface connector (CN2) is FI-SEB20P-HF13E-E1500 made by JAE or equivalent connector and pin assignment is as below:

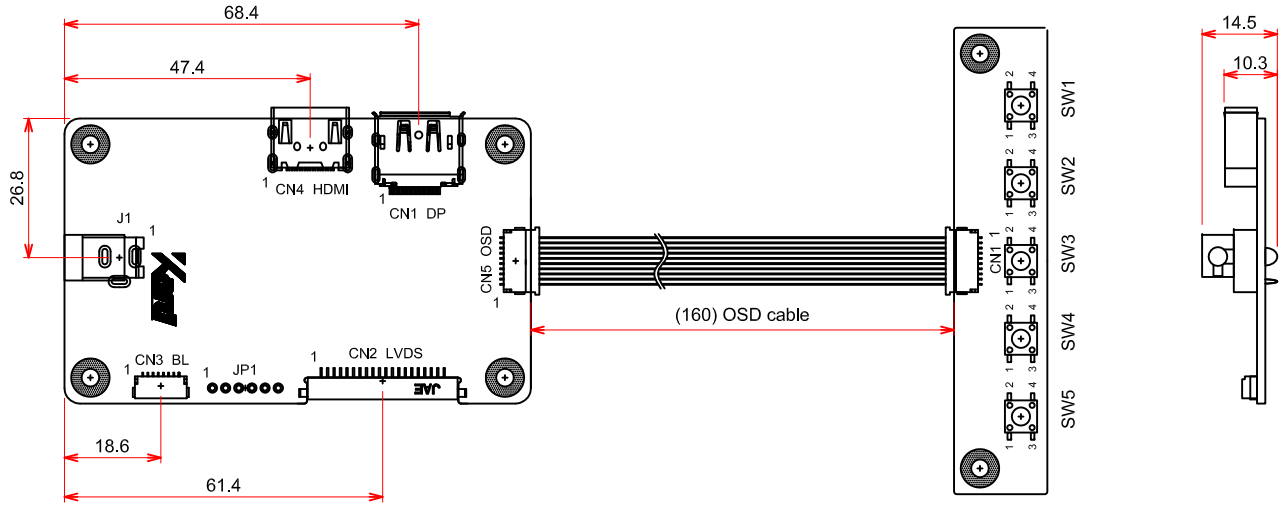
Item	Pin No.	Signal	Function
CN2 (LVDS)	1	VDD (3.3V)	Power supply for logic
	2	VDD (3.3V)	Power supply for logic
	3	GND	GND
	4	GND	GND
	5	IN0-	LVDS data pair (R0~R5, G0)
	6	IN0+	
	7	GND	GND
	8	IN1-	LVDS data pair (G1~G5, B0~B1)
	9	IN1+	
	10	GND	GND
	11	IN2-	LVDS data pair (B2~B5, DE)
	12	IN2+	
	13	GND	GND
	14	CLK IN-	LVDS data pair (Pixel Clock)
	15	CLK IN+	
	16	GND	GND
	17	IN3-	LVDS data pair (R6~R7, G6~G7, B6~B7)
	18	IN3+	
	19	NC	No connection
	20	Dim	Brightness dimming (Note1)

Note 1: Normal brightness: 0% PWM duty; Brightness control: 0% to 100% PWM duty.

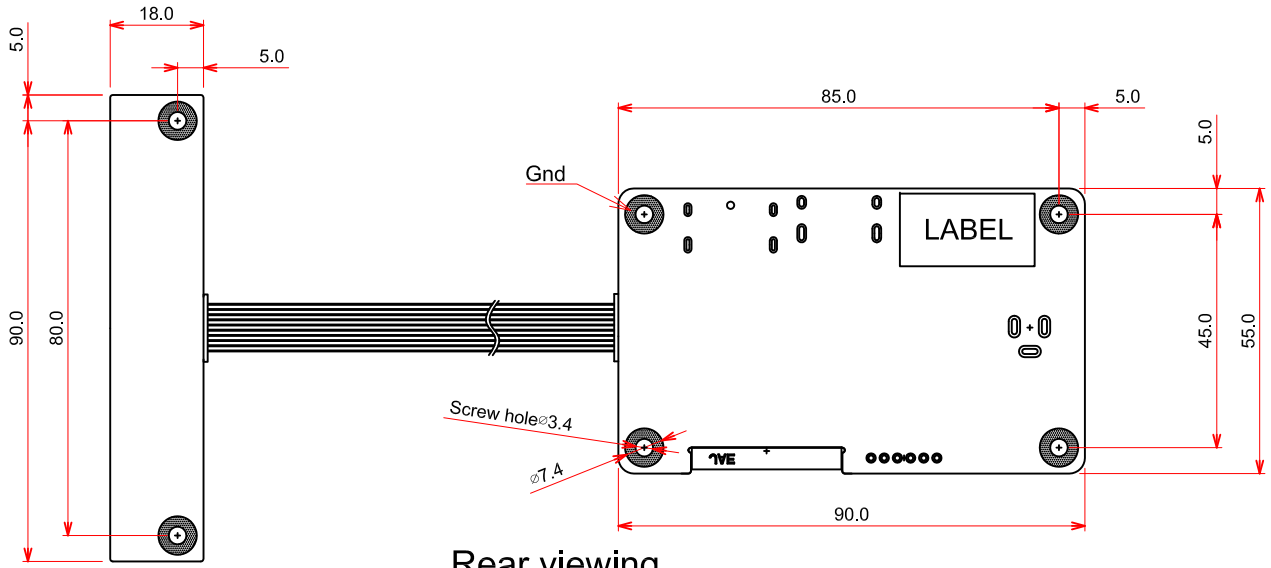
The display interface connector (CN3) is SM08 B-SRSS-TB made by JST or equivalent connector and pin assignment is as below:

Item	Pin No.	Signal	Function
CN3	1	VLED (+) (12V)	Power supply for Backlight
	2	VLED (+) (12V)	Power supply for Backlight
	3	VLED (+) (12V)	Power supply for Backlight
	4	VLED (-)	GND
	5	VLED (-)	GND
	6	VLED (-)	GND
	7	NC	No connection
	8	NC	No connection

8. OUTLINE DIMENSIONS



Front viewing



Rear viewing

General Tolerance:±0.5mm
Scale : NTS
Unit : mm

JDI Taiwan Inc. Kaohsiung Branch	SHEET No.	7B64PS 2708-ADB31200-2	PAGE	8-1/1

9. DESIGNATION OF LOT MARK

1) The lot mark is showing in Fig.9.1. First 4 digits are used to represent production lot, T represented made in Taiwan, and the last 6 digits are the serial number.

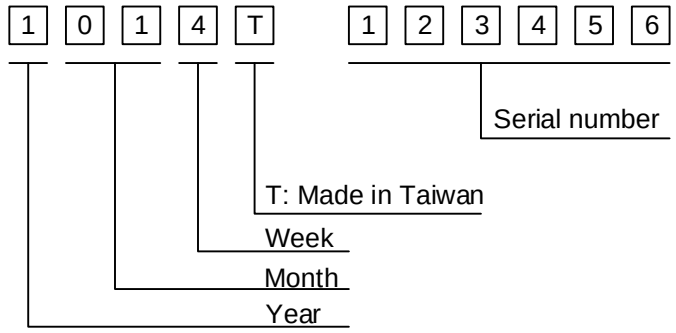


Fig. 9.1

2) The tables as below are showing what the first 4 digits of lot mark are shorted for.

Year	Lot Mark
2021	1
2022	2
2023	3
2024	4
2025	5

Month	Lot Mark	Month	Lot Mark
Jan.	01	Jul.	07
Feb.	02	Aug.	08
Mar.	03	Sep.	09
Apr.	04	Oct.	10
May	05	Nov.	11
Jun.	06	Dec.	12

Week	Lot Mark
1~7 days	1
8~14 days	2
15~21 days	3
22~28 days	4
29~31 days	5

3) Except letters I and O, revision number will be shown on lot mark and following letters A to Z.

4) The location of the lot mark is on the back of the display shown in Fig. 9.2.

Label example:



Fig. 9.2